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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,286	07/30/2003	Robert T. George	ITL.1034US (P16844)	9710

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EXAMINER	
PATEL, NIKETA I	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/630,286	GEORGE ET AL.	
	Examiner	Art Unit	
	Niketa I. Patel	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5,6,8,10,11,13,14,16,17,20,22-24,32 and 34-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,6,8,10,11,13,14,16,17,20,22-24,32 and 34-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/30/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

NIP 3/26/08

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 6, 7, 17, 20, 23, 24, 32, 34-42 are rejected under 35 U.S.C. 102(b) as being anticipate by Sindhu U.S. Patent Number: 5,230,045 (hereinafter "*Sindhu*".)

3. **Referring to claims 1, 20**, *Sindhu* teaches an apparatus comprising: a pipeline resource [see column 4, lines 6-21 – map cache 58] having a plurality of address spaces [see column 3, lines 19-31 – multiple address space and column 4, lines 6-21], each of the plurality of address spaces corresponding to one of a plurality of address space identifiers [see column 3, lines 19-31 – address space identifier], the pipeline resource including entries each including one of the plurality of address space identifiers [see column 4, lines 6-21 and column 6, lines 41-52 and column 12, lines 21-35, plurality of entries of map cache 58], wherein the entries are selectively flushable on an address space basis [see column 15, lines 65-67 and column 16, lines 1-15 – Flush-Entry command with an AID (address space identifier)]; and a filter coupled to the pipeline resource to select at least one of the entries of the pipeline resource to be flushed, the filter to cause one of the plurality of address spaces in the pipeline resource to be flushed while

the other address spaces are maintained [see column 16, lines 3-14 – examiner equates filter with matching.]

4. **Referring to claims 3, 17**, *Sindhu* teaches further comprising a control register coupled to the pipeline resource to provide the plurality of address space identifiers to the entries [see figure 4, element 118 – central control.]

5. **Referring to claim 6**, *Sindhu* teaches wherein the pipeline resource comprises a translation lookaside buffer [see column 4, lines 6-21 – address translation cache.]

6. **Referring to claim 7**, *Sindhu* teaches further comprising a filter coupled to the translation lookaside buffer to select at least one of the entries to be flushed [see column 15, lines 65-67 and column 16, lines 1-15 – Flush-Entry command with an AID (address space identifier).]

7. **Referring to claim 23,** *Sindhu* teaches further comprising instructions that if executed enable the system to associate a different address space identifier with a second value, the different address space identifier corresponding to a different active context than the address space identifier [see column 10, lines 47-63 – shared AID.]

8. **Referring to claim 24**, *Sindhu* teaches further comprising instructions that if executed enable the system to invalidate the entry if the value is updated during a context [see column 15, lines 65-67 and column 16, lines 1-15 – Flush-Entry command with an AID (address space identifier).]

9. **Referring to claim 32**, *Sindhu* teaches further comprising instructions that if executed enable the system to flush the portion of the pipeline resource on a next context switch after the

invalidation [see column 15, lines 65-67 and column 16, lines 1-15 – Flush-Entry command with an AID (address space identifier).]

10. **Referring to claim 34,** *Sindhu* teaches wherein the filter is to store a plurality of filter entries each including a pair of valid indicators, an address space identifier, and a thread identifier [see column 15, lines 65-67 and column 16, lines 1-15 – Flush-Entry command with an AID (address space identifier).]

11. **Referring to claim 35,** *Sindhu* teaches wherein the first valid indicator of a filter entry is to be written if no conflicting invalidity access occurs on an address match to the filter entry and the second valid indicator of the filter entry is to be written if a conflicting invalidity access occurs on the address match [see column 15, lines 65-67 and column 16, lines 1-15 – Flush-Entry command with an AID (address space identifier).]

12. **Referring to claim 36,** *Sindhu* teaches further comprising a control register coupled to the filter, the control register having an entry for each entry of the filter, wherein a control register entry is to be updated if art address matches the corresponding entry of the filter [see column 15, lines 65-67 and column 16, lines 1-15 – Flush-Entry command with an AID (address space identifier).]

13. **Referring to claim 37,** *Sindhu* teaches wherein the address is a post-retirement store address [see column 15, lines 65-67 and column 16, lines 1-15 – Flush-Entry command with an AID (address space identifier).]

14. **Referring to claim 38,** *Sindhu* teaches wherein the filter is to store a plurality of filter entries each including an address space identifier and a thread identifier [see column 15, lines 65-67 and column 16, lines 1-15 – Flush-Entry command with an AID (address space identifier).]

15. **Referring to claim 39**, *Sindhu* teaches wherein the plurality of filter entries are to further each include a pair of valid indicators [see column 15, lines 65-67 and column 16, lines 1-15 – Flush-Entry command with an AID (address space identifier).]

16. **Referring to claim 40**, *Sindhu* teaches wherein the first valid indicator of a filter entry is to be written if no conflicting invalidity access occurs on an address match to the filter entry and the second valid indicator of the filter entry is to be written in a conflicting invalidity access occurs on the address match [see column 15, lines 65-67 and column 16, lines 1-15 – Flush-Entry command with an AID (address space identifier).]

17. **Referring to claim 41**, *Sindhu* teaches further comprising a second control register coupled to the filter, the second control register having an entry for each entry of the filter, wherein the second control register entry is to be updated if an address matches the corresponding entry of the filter[see column 15, lines 65-67 and column 16, lines 1-15 – Flush-Entry command with an AID (address space identifier).]

18. **Referring to claim 42**, *Sindhu* teaches wherein the address is a post-retirement store address [see column 15, lines 65-67 and column 16, lines 1-15 – Flush-Entry command with an AID (address space identifier).]

19. Claims 8-9, 14, 16-17, 25, 29-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishikawa et al. U.S. Patent Application Publication No.: 2004/0193778 A1 (hereinafter "*Ishikawa*".)

20. **Referring to claims 8, 25**, *Ishikawa* teaches a method comprising: associating an address space identifier with a value; hashing the address space identifier with a portion of the value [see

paragraph 10 and 60 – TLB entries, address space identifiers, hash processed]; and thereafter storing the value and the address space identifier in a pipeline resource [see paragraph 10 and 60 – TLB entries, address space identifiers, hash processed.]

21. **Referring to claim 9**, *Ishikawa* teaches a method further comprising storing the value and the address space identifier in an entry of the pipeline resource [see paragraph 10 and 60 – TLB entries, address space identifiers, hash processed.]

22. **Referring to claims 14, 30, 29**, *Ishikawa* teaches a method further comprising associating a second address space identifier with a second value; and storing the second value and the second address space identifier in the pipeline resource [see paragraph 10 and 60 – TLB entries, address space identifiers, hash processed.]

23. **Referring to claim 16**, *Ishikawa* teaches system comprising: a processor including a pipeline resource [see paragraph 10 and 60 – TLB] including a plurality of entries each having one of a plurality of address spaces [see paragraph 10 and 60 – TLB, address space identifiers], each of the plurality of address spaces corresponding to one of a plurality of address space identifiers [see paragraph 10 and 60 – TLB, address space identifiers]; a hashing engine to hash one of the plurality of address space identifiers with a portion of a value to be stored in one of the entries [see paragraph 10 and 60 – TLB, address space identifiers, hash]; and a dynamic random access memory coupled to the processor [see paragraph 33, memories.]

24. **Referring to claim 17**, *Ishikawa* teaches further comprising a control register coupled to the pipeline resource to provide the plurality of address space identifiers to the pipeline resource [see figure 11, elements 1011, 1005, 1006.]

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 5 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nozue et al. U.S. Patent Number: 5,627,987 (hereinafter "*Nozue*".)

27. **Referring to claims 5, 22,** *Sindhu* teaches the limitations set forth above however is silent regarding the limitation of wherein the entries further include a thread identifier [see column 23, lines 54-67, TLB with thread numbers] in order to provide physical page numbers associated with a thread.

One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous for the TLB to include entering having a thread identifier stored there on in order to provide physical page numbers associated with a thread. It is for this reason that one of ordinary skill in the art would have been motivated to implement a TLB with thread identifiers to provide physical page numbers associated with a thread.

28. Claims 10 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Ishikawa* and further in view of Zuraski, Jr. et al U.S. Patent Number: 6,510,508 B1 (hereinafter "*Zuraski*".)

29. **Referring to claims 10, 27,** teaches the limitations set forth above however, does not set forth the limitation of further comprising invalidating the entry if an update to the value occurs

during a context. *Zuraski* teaches this limitation [see *Zuraski* column 13, lines 4-11] in order to avoid use of stale data and thereby preventing system failure.

One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous for the system to invalidate an entry if an update to the value occurs during a context in order to avoid use of stale data and thereby preventing system failure. It is for this reason that one of ordinary skill in the art would have been motivated to implement invalidating the entry if an update to the value occurs during a context to avoid use of stale data and thereby preventing system failure.

30. Claims 11-13 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Ishikawa*, *Zuraski* and further in view of *Sindhu*.

31. **Referring to claims 11, 12, 13, 33**, the combination of *Ishikawa* and *Zuraski* discloses the limitation of flushing the invalidated entry [see *Zuraski* column 13, lines 4-11] however does not set forth the limitation of selectively flushing the entry. *Sindhu* teaches to selectively flush an entry [see column 15, lines 65-67 and column 16, lines 1-15 – Flush-Entry command with an AID (address space identifier)] in order to improve system performance.

One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous to selectively flash an entry in order to improve system performance. It is for this reason that one of ordinary skill in the art would have been motivated to implement the limitation of selectively flushing the entry in order to improve system performance.

Response to Arguments

32. Applicant's arguments filed 9/12/2007 have been fully considered but they are not persuasive. The applicant argues that *Sindhu* does not teach the limitation of a filter coupled to the pipeline resource to select at least one of the entries of the pipeline resource to be flushed, the filter to cause one of the plurality of address spaces in the pipeline resource to be flushed while the other address spaces are maintained.

The examiner respectfully disagrees with this argument. *Sindhu* teaches the limitation of a filter coupled to the pipeline resource to select at least one of the entries of the pipeline resource to be flushed, the filter to cause one of the plurality of address spaces in the pipeline resource to be flushed while the other address spaces are maintained [see column 16, lines 3-14 – examiner equates filter with matching.]

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Niketa I. Patel whose telephone number is (571) 272 4156. The examiner can normally be reached on M-F 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272 4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Niketa Patel
Patent Examiner
AU 2181